REMARKS/ARGUMENTS

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and the following remarks are presented for the Examiner's consideration.

Claims 1-3, 5-7, 12-14 and 16-18 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,136,376 to Yagasaki et al. (hereinafter "Yagasaki"). For the following reasons, Applicants respectfully request the Examiner's reconsideration of the claims.

Regarding claims 1 and 12, Applicants previously argued that Yagasaki does not teach a controller for controlling the operation of the video compression unit *and the video transmission unit*, as required. In the "Response to Arguments" section of the Office action, the Examiner responded by asserting, *inter alia*, that Yagasaki utilizes "a commonly well known MPEG video encoding scheme, the recursive buffer quantization scheme" such that "the quantization rate controller or Yagasaki's data control circuit 31 acts as a medium to interactively affect the coding rate and the transmission rate." Thus, the Examiner has apparently concluded that, due to its control of the video compression rate, the data control circuit (31) indirectly affects the transmission speed of the transmission buffer memory (3) to the transmission path (4), thereby satisfying the above-mentioned limitations of claims 1 and 12.

Applicant respectfully submits that, with reference to Fig.2, Yagasaki clearly indicates that the transmission buffer memory (3) transmits the transmission data (D_{TRANS}) at a transmitting velocity (speed) determined by the transmission capacity of the transmission path (4), which is independent of operation of the video signal coding circuit (2) (column 1, line 52 to column 2, line 11). Put another way, the transmission data D_{TRANS} will be transmitted by the transmission buffer memory (3) to the transmission path (4) at a speed dictated by the available bandwidth in the transmission path (4), regardless of the rate of compression of the video data (VD) into coded data (D_{VD}) *and* regardless of the rate of transmission of the coded data (D_{VD}) into the transmission buffer memory (3). Thus, in Yagasaki, the data control circuit (31) of the video signal encoding circuit (2) only supplies data to the transmission buffer memory (3), but does not control how the transmission buffer memory (3) operates on that data.

Further, regarding claims 1 and 12, even if, for purposes of this argument, due to its control of the video compression rate, the data control circuit (31) is considered to indirectly affect the operation of the transmission buffer memory (3), not every limitation of the claims would be taught. In particular, there would still be no teaching in Yagasaki that the video compression unit and the video transmission unit were operated in parallel, as required by claims 1 and 12. That is, according to the Examiner's interpretation of Yagasaki, the data control circuit (31) must first affect the operation of the video signal encoding circuit (2) before it can affect the operation of the transmission buffer memory (3). Thus, the video signal encoding circuit (2) and the transmission buffer memory (3) would be operated in a serial fashion, not in parallel as required by the claims.

Moreover, the claimed parallel operation of the compression unit and the video transmission unit is not possible according to the disclosure of Yagasaki. As explained in the specification at pages 12-14, in order for the video compression unit and the video transmission unit to be operated in parallel by the controller, the controller identifies the time required for transmission and controls the encoding by the compression unit to compress the video as much as possible within the given time, thereby controlling the time required for encoding so that is less than the time for transmission, making the above-mentioned parallel operation possible. However, the data control circuit (31) of Yagasaki is merely providing feedback to the encoding circuit (2) to generate the data having a particular transmission rate, which corresponds to the required time for *transmitting*. That is, the data control circuit of Yagasaki control the transmission rate, but does not control the required time for *encoding*, as in the present invention.

For all of the above reasons, every limitation of claims 1 and 12 is not taught by Yagasaki. Therefore, claims 1 and 12, and their respective dependent claims 2, 3, 5-7, 13, 14 and 16-18, are not anticipated by Yagasaki.

Claim 4 and 15 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yagasaki in view of U.S. Patent No. 5,638,129 to Lee (hereinafter "Lee"), and claims 9-10 and 20-21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yagasaki in view of U.S. Patent No. 5,537,409 to Moriyama (hereinafter "Moriyama"). For the reasons explained above, Yagasaki does not teach or

suggest every limitation of the claims. Further, neither Lee nor Moriyama teach or suggest the limitations of which Yagasaki is deficient, namely a controller for controlling the operation of the video compression unit and the video transmission unit, and the serial operation thereof. Therefore, since every limitation of the claim is not taught or suggested by the references as required, claims 4, 9, 10, 15, 20 and 21 are patentable over the prior art of record.

In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. 33826.

Respectfully submitted,

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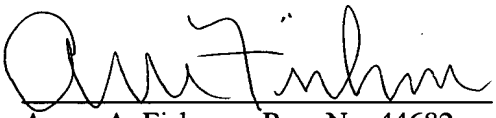
By: 
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